

DATA SHEET

74ABT16646

74ABTH16646

16-bit bus transceiver/register (3-State)

Product specification
Supersedes data of 1995 Aug 17
IC23 Data Handbook

1998 Feb 27

16-bit bus transceiver/register (3-State)

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FEATURES

- Independent registers for A and B buses
- Multiple V_{CC} and GND pins minimize switching noise
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- Multiplexed real-time and stored data
- Outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per JEDEC Std 17
- 74ABTH16646 incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ABT16646 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16646 16-bit transceiver/register consists of two sets of bus transceiver circuits with 3-State outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (\overline{nOE}) and Direction (\overline{nDIR}) pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (\overline{nSAB} , \overline{nSBA}) pins determine whether data is stored or transferred through the device in real-time. The \overline{nDIR} determines which bus will receive data when the \overline{nOE} is active Low. In the isolation mode (\overline{nOE} = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B may be driven at a time.

Two options are available, 74ABT16646 which does not have the bus-hold feature and 74ABTH16646 which incorporates the bus-hold feature.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0V | TYPICAL | UNIT |
|------------------------|---------------------------------|---|------------|---------------|
| t_{PLH} t_{PHL} | Propagation delay nAx to nBx | $C_L = 50\text{pF}$; $V_{CC} = 5\text{V}$ | 3.3 2.7 | ns |
| C_{IN} | Input capacitance | $V_I = 0\text{V}$ or V_{CC} | 3 | pF |
| $C_{I/O}$ | I/O capacitance | $V_O = 0\text{V}$ or V_{CC} ; 3-State | 7 | pF |
| I_{CCZ} | Quiescent supply current | Outputs disabled; $V_{CC} = 5.5\text{V}$ | 550 | μA |
| | | Outputs low; $V_{CC} = 5.5\text{V}$ | 9 | mA |

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|--|-----------------------|---------------|------------|
| 56-Pin Plastic SSOP Type III | -40°C to $+85^{\circ}\text{C}$ | 74ABT16646 DL | BT16646 DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | -40°C to $+85^{\circ}\text{C}$ | 74ABT16646 DGG | BT16646 DGG | SOT364-1 |
| 56-Pin Plastic SSOP Type III | -40°C to $+85^{\circ}\text{C}$ | 74ABTH16646 DL | BH16646 DL | SOT371-1 |
| 56-Pin Plastic TSSOP Type II | -40°C to $+85^{\circ}\text{C}$ | 74ABTH16646 DGG | BH16646 DGG | SOT364-1 |

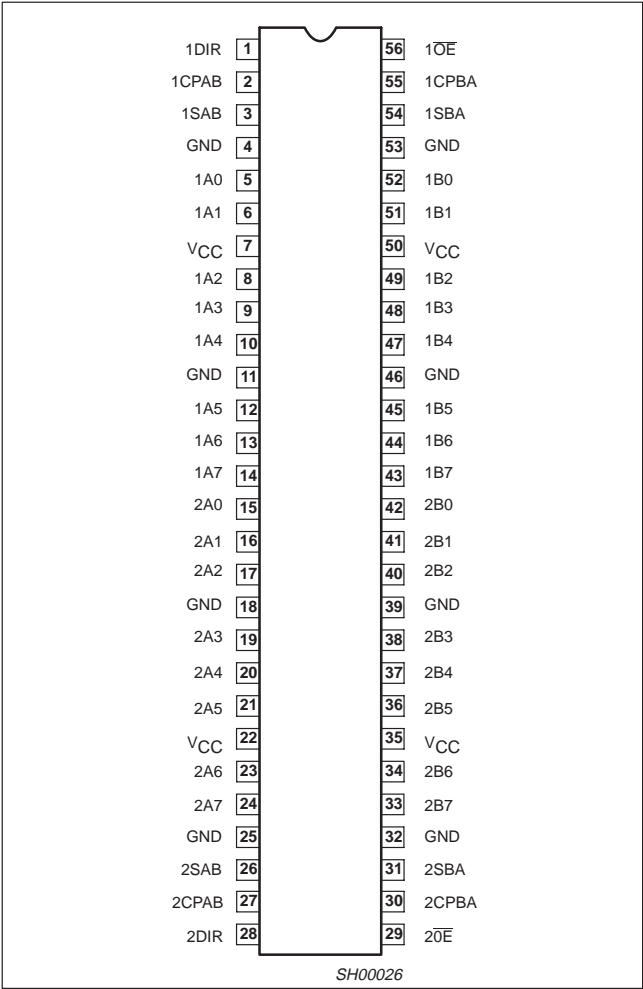
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|--|-------------------------------------|---|
| 2, 55, 27, 30 | 1CPAB, 1CPBA, 2CPAB, 2CPBA | Clock input A to B / Clock input B to A |
| 3, 54, 26, 31 | 1SAB, 1SBA, 2SAB, 2SBA | Select input A to B / Select input B to A |
| 1, 28 | 1DIR, 2DIR | Direction control inputs |
| 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24 | 1A0 – 1A7, 2A0 – 2A7 | Data inputs/outputs (A side) |
| 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33 | 1B0 – 1B7, 2B0 – 2B7 | Data inputs/outputs (B side) |
| 56, 29 | $1\overline{OE}$, $2\overline{OE}$ | Output enable inputs |
| 4, 11, 18, 25, 32, 39, 46, 53 | GND | Ground (0V) |
| 7, 22, 35, 50 | V_{CC} | Positive supply voltage |

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PIN CONFIGURATION



FUNCTION TABLE

| INPUTS | | | | | | DATA I/O | | OPERATING MODE |
|--------------------------|--------|----------------------|----------------------|--------|--------|---------------------|---------------------|---|
| n $\overline{\text{OE}}$ | nDIR | nCPAB | nCPBA | nSAB | nSBA | nAx | nBx | |
| X | X | \uparrow | X | X | X | Input | Unspecified output* | Store A, B unspecified |
| X | X | X | \uparrow | X | X | Unspecified output* | Input | Store B, A unspecified |
| H H | X X | \uparrow H or L | \uparrow H or L | X X | X X | Input | Input | Store A and B data Isolation, hold storage |
| L L | L L | X X | X H or L | X X | L H | Output | Input | Real time B data to A bus Stored B data to A bus |
| L L | H H | X H or L | X X | L H | X X | Input | Output | Real time A data to B bus Stored A data to B bus |

H = High voltage level

L = Low voltage level

X = Don't care

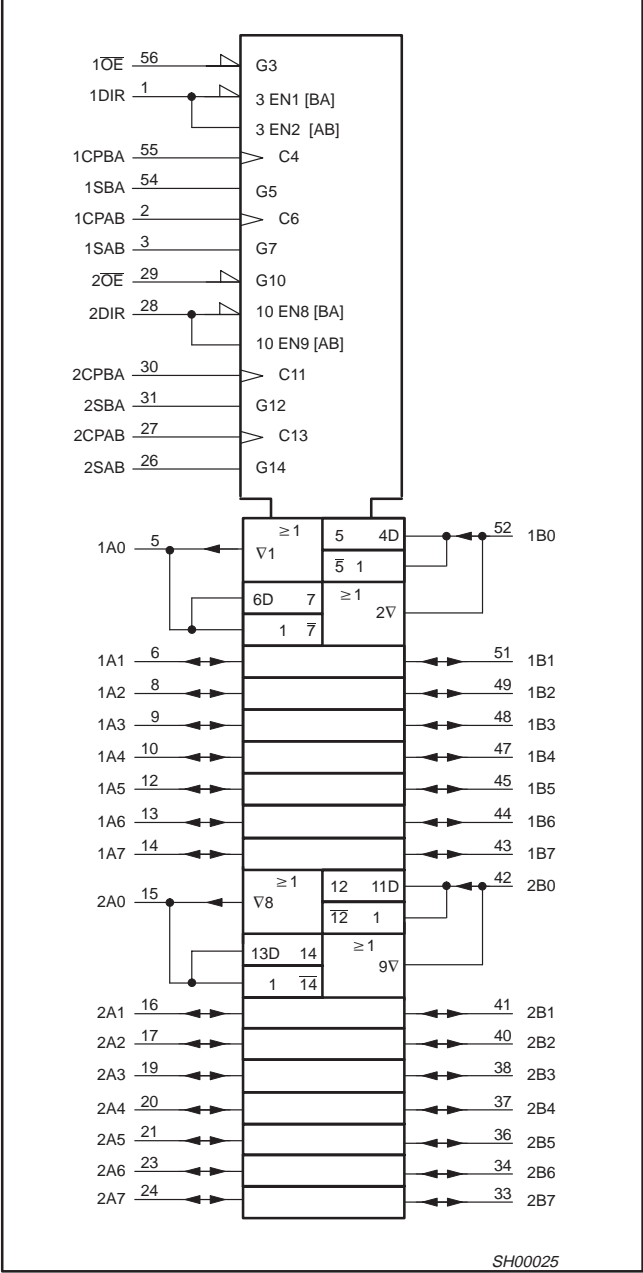
\uparrow = Low-to-High clock transition

* The data output function may be enabled or disabled by various signals at the n $\overline{\text{OE}}$ input. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

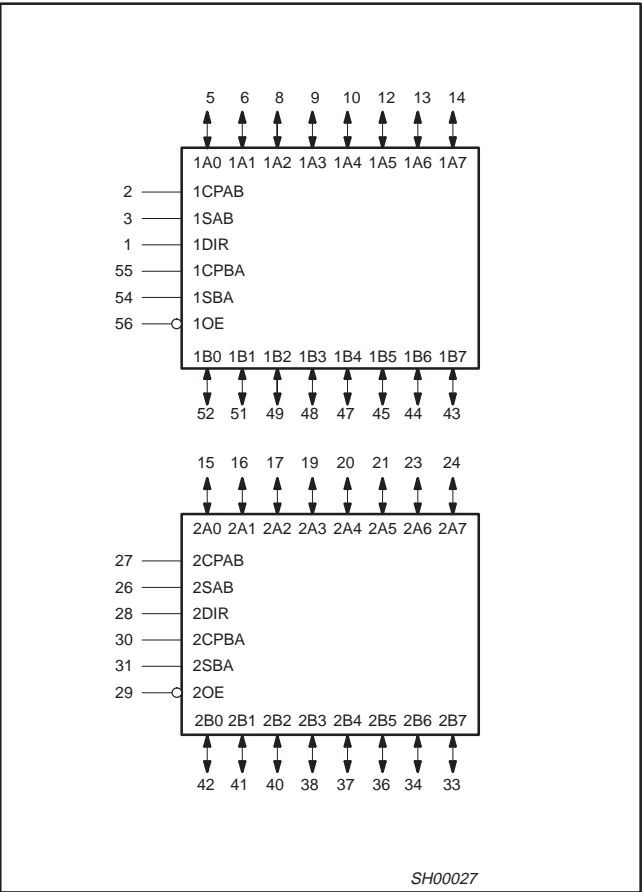
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LOGIC SYMBOL (IEEE/IEC)



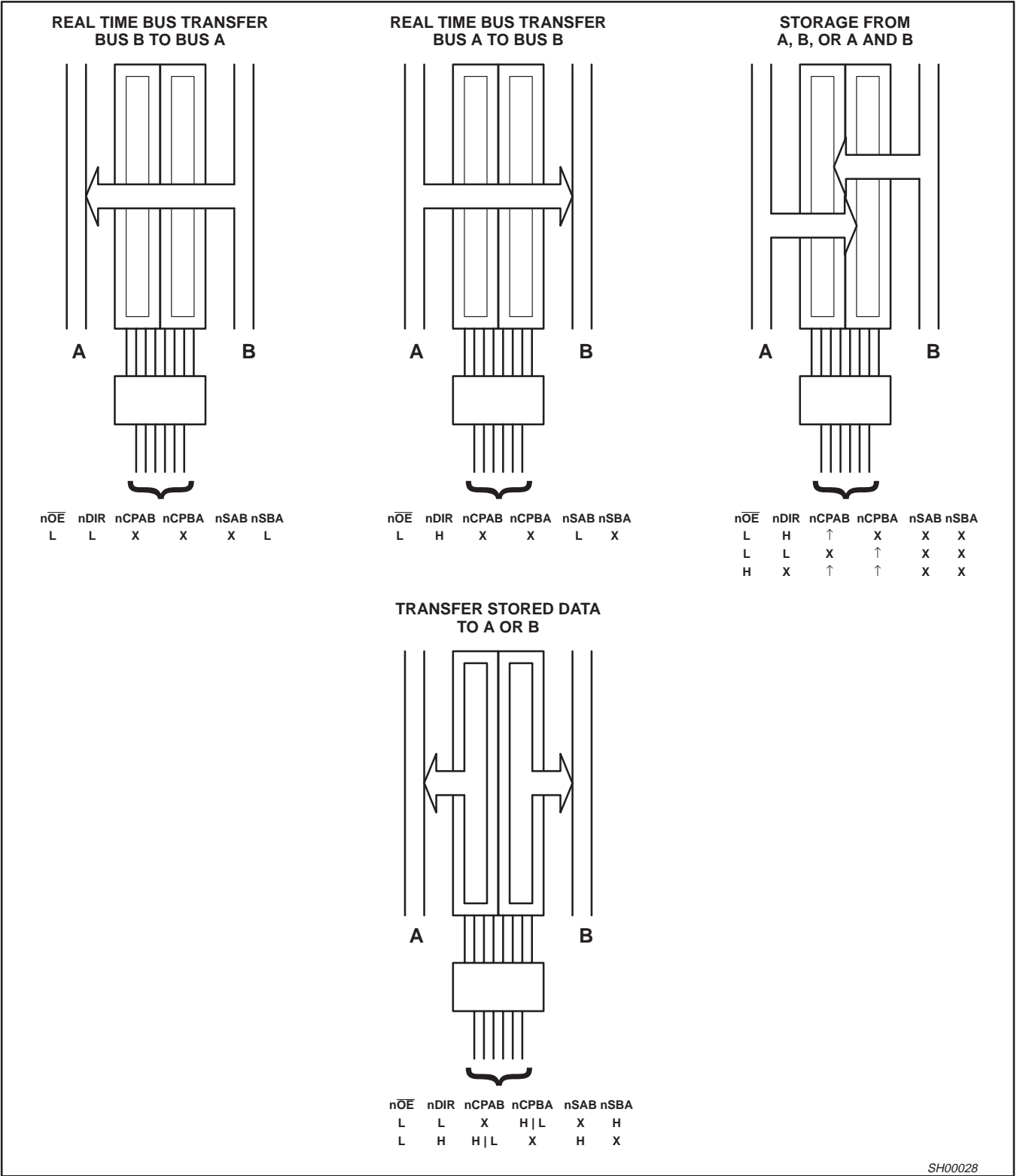
LOGIC SYMBOL



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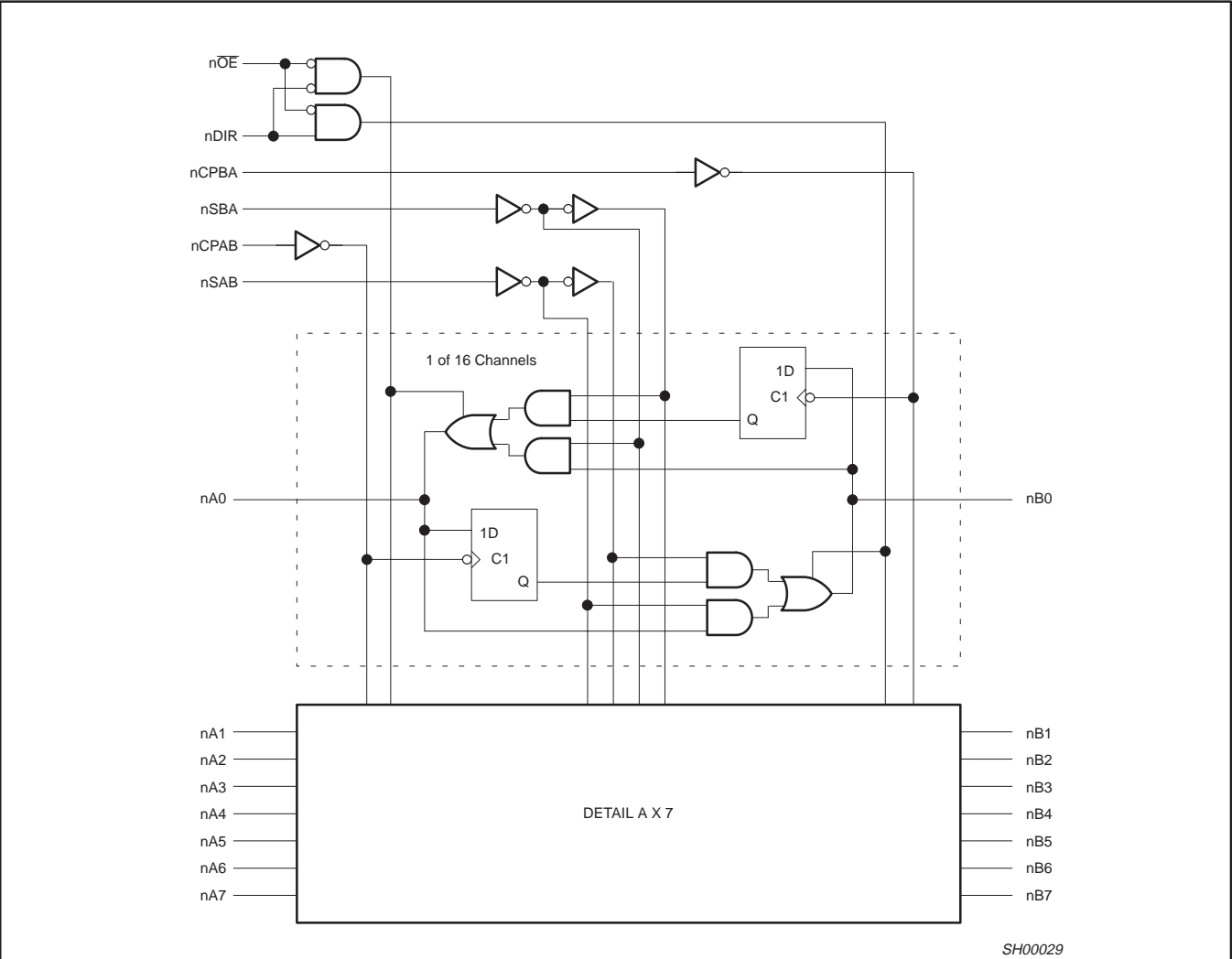
The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT16646.



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LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS^{1, 2}

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------|--------------------------------|-----------------------------|--------------|------|
| V _{CC} | DC supply voltage | | −0.5 to +7.0 | V |
| I _{IK} | DC input diode current | V _I < 0 | −18 | mA |
| V _I | DC input voltage ³ | | −1.2 to +7.0 | V |
| I _{OK} | DC output diode current | V _O < 0 | −50 | mA |
| V _{OUT} | DC output voltage ³ | output in Off or High state | −0.5 to +5.5 | V |
| I _{OUT} | DC output current | output in Low state | 128 | mA |
| | | output in High state | −64 | mA |
| T _{stg} | Storage temperature range | | −65 to 150 | °C |

- NOTES:**
- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
 - The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
 - The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | UNIT |
|---------------------|--------------------------------------|--------|----------|------|
| | | MIN | MAX | |
| V_{CC} | DC supply voltage | 4.5 | 5.5 | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_{IH} | High-level input voltage | 2.0 | | V |
| V_{IL} | Low-level Input voltage | | 0.8 | V |
| I_{OH} | High-level output current | | -32 | mA |
| I_{OL} | Low-level output current | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| T_{amb} | Operating free-air temperature range | -40 | +85 | °C |

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT | |
|------------------------------------|--|--|--------------------------|------|-------|-----------------------------------|-----|------|----|
| | | | T _{amb} = +25°C | | | T _{amb} = -40°C to +85°C | | | |
| | | | MIN | TYP | MAX | MIN | MAX | | |
| V _{IK} | Input clamp voltage | V _{CC} = 4.5V; I _{IK} = -18mA | | | -0.9 | -1.2 | | -1.2 | V |
| V _{OH} | High-level output voltage | V _{CC} = 4.5V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | | 2.5 | 2.9 | | 2.5 | | V |
| | | V _{CC} = 5.0V; I _{OH} = -3mA; V _I = V _{IL} or V _{IH} | | 3.0 | 3.4 | | 3.0 | | V |
| | | V _{CC} = 4.5V; I _{OH} = -32mA; V _I = V _{IL} or V _{IH} | | 2.0 | 2.4 | | 2.0 | | V |
| V _{OL} | Low-level output voltage | V _{CC} = 4.5V; I _{OL} = 64mA; V _I = V _{IL} or V _{IH} | | | 0.35 | 0.55 | | 0.55 | V |
| V _{RST} | Power-up output voltage ³ | V _{CC} = 5.5V; I _O = 1mA; V _I = GND or V _{CC} | | | 0.13 | 0.55 | | 0.55 | V |
| I _I | Input leakage current | V _{CC} = 5.5V; V _I = GND or 5.5V | Control pins | | ±0.01 | ±1.0 | | ±1.0 | μA |
| I _{HOLD} | Bus Hold current A or B Ports ⁵ 74ABTH16646 | V _{CC} = 4.5V; V _I = 0.8V | | 35 | | | 35 | | μA |
| | | V _{CC} = 4.5V; V _I = 2.0V | | -75 | | | -75 | | |
| | | V _{CC} = 5.5V; V _I = 0 to 5.5V | | ±800 | | | | | |
| I _{OFF} | Power-off leakage current | V _{CC} = 0.0V; V _O = 4.5V; V _I = 0.0V or 5.5V | | | ±2.0 | ±100 | | ±100 | μA |
| I _{PU/PD} | Power-up/down 3-State output current ⁴ | V _{CC} = 2.1V; V _O = 0.0V or V _{CC} ; V _I = GND or V _{CC} ; OE/OE = X | | | ±1.0 | ±50 | | ±50 | μA |
| I _{IH} + I _{OZH} | 3-State output High current | V _{CC} = 5.5V; V _O = 5.5V; V _I = V _{IL} or V _{IH} | | | 1.0 | 10 | | 10 | μA |
| I _{IL} + I _{OZL} | 3-State output Low current | V _{CC} = 5.5V; V _O = 0.0V; V _I = V _{IL} or V _{IH} | | | -1.0 | -10 | | -10 | μA |
| I _{CEX} | Output High leakage current | V _{CC} = 5.5V; V _O = 5.5V; V _I = GND or V _{CC} | | | 5.0 | 50 | | 50 | μA |
| I _O | Output current ¹ | V _{CC} = 5.5V; V _O = 2.5V | | -50 | -80 | -180 | -50 | -180 | mA |
| I _{CCH} | Quiescent supply current | V _{CC} = 5.5V; Outputs High, V _I = GND or V _{CC} | | | 0.55 | 2 | | 2 | mA |
| I _{CCL} | | V _{CC} = 5.5V; Outputs Low, V _I = GND or V _{CC} | | | 9 | 19 | | 19 | mA |
| I _{CCZ} | | V _{CC} = 5.5V; Outputs 3-State; V _I = GND or V _{CC} | | | 0.55 | 2 | | 2 | mA |
| ΔI _{CC} | Additional supply current per input pin ² 74ABT16646 | V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND | | | 5.0 | 50 | | 50 | μA |
| ΔI _{CC} | Additional supply current per input pin ² 74ABTH16646 | V _{CC} = 5.5V; one input at 3.4V, other inputs at V _{CC} or GND | | | 200 | 500 | | 500 | μA |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V_{CC} between 0V and 2.0V, with a transition time of up to 100msec. From $V_{CC} = 2.1\text{V}$ to $V_{CC} = 5\text{V} \pm 10\%$ a transition time of up to 100 μsec is permitted.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

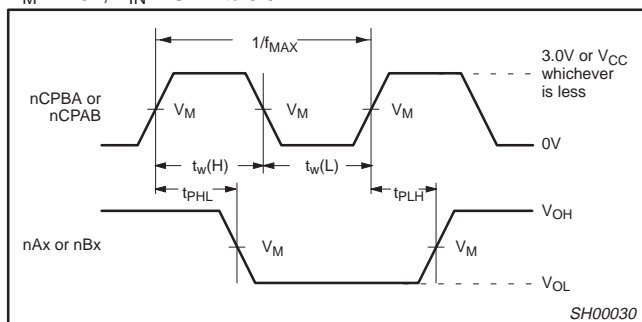
| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | UNIT |
|--------------------------------------|---|----------|---|------------|------------|--|------------|------|
| | | | T _{amb} = +25°C V _{CC} = +5.0V | | | T _{amb} = -40 to +85°C V _{CC} = +5.0V ±0.5V | | |
| | | | MIN | TYP | MAX | MIN | MAX | |
| f _{MAX} | Maximum clock frequency | 1 | 125 | | | 125 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay nCPAB to nBx or nCPBA to nAx | 1 | 1.5 1.5 | 3.3 2.7 | 4.0 4.1 | 1.5 1.5 | 4.9 4.7 | ns |
| t _{PLH} t _{PHL} | Propagation delay nAx to nBx or nBx to nAx | 2 | 1.0 1.0 | 2.3 2.0 | 3.2 4.1 | 1.0 1.0 | 3.9 4.6 | ns |
| t _{PLH} t _{PHL} | Propagation delay nSAB to nBx or nSBA to nAx | 2, 3 | 1.0 1.0 | 3.1 2.7 | 4.3 4.3 | 1.0 1.0 | 5.0 5.0 | ns |
| t _{PZH} t _{PZL} | Output enable time nOE to nAx or nBx | 5, 6 | 1.0 1.5 | 3.2 3.3 | 4.6 4.9 | 1.0 1.5 | 5.5 5.7 | ns |
| t _{PHZ} t _{PLZ} | Output disable time nOE to nAx or nBx | 5, 6 | 1.5 1.5 | 3.5 2.7 | 4.9 4.1 | 1.5 1.5 | 5.4 4.5 | ns |
| t _{PZH} t _{PZL} | Output enable time nDIR to nAx or nBx | 5, 6 | 1.0 1.5 | 4.1 4.3 | 4.8 4.8 | 1.0 1.5 | 5.4 5.6 | ns |
| t _{PHZ} t _{PLZ} | Output disable time nDIR to nAx or nBx | 5, 6 | 2.0 1.5 | 3.6 2.7 | 5.7 5.1 | 2.0 1.5 | 6.7 5.9 | ns |

AC SETUP REQUIREMENTS

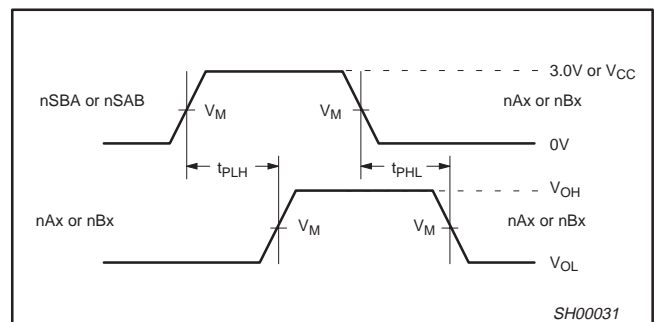
GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|------------------------------------|--|----------|--|-------------|--|------|
| | | | $T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$ | | $T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$ | |
| | | | MIN | TYP | MIN | |
| $t_s(\text{H})$ $t_s(\text{L})$ | Setup time nAx to nCPAB, nBx to nCPBA | 4 | 2.0 1.5 | 1.0 0.8 | 2.0 1.5 | ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time nAx to nCPAB, nBx to nCPBA | 4 | 1.5 1.0 | 0.0 -0.7 | 1.5 1.0 | ns |
| $t_w(\text{H})$ $t_w(\text{L})$ | Pulse width, High or Low nCPAB or nCPBA | 1 | 4.5 3.0 | 2.5 2.0 | 4.5 3.0 | ns |

AC WAVEFORMS

 $V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$ 

Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



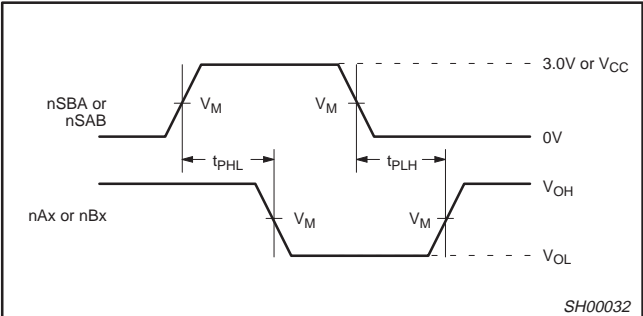
Waveform 2. Propagation Delay, nSAB to nBx or nSBA to nAx, nAx to nBx or nBx to nAx

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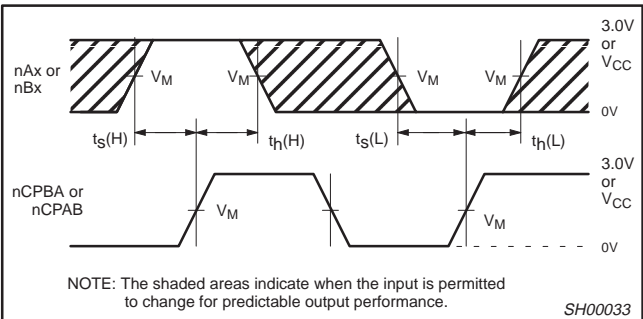
74ABT16646
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AC WAVEFORMS (Continued)

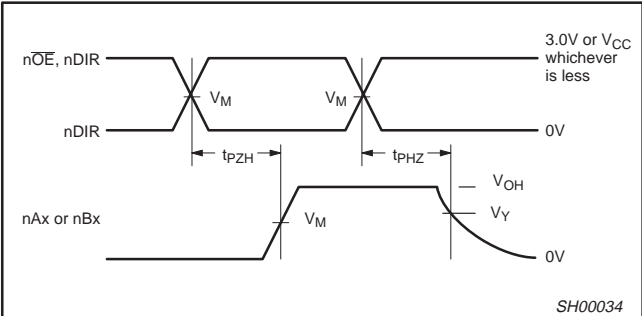
$V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$



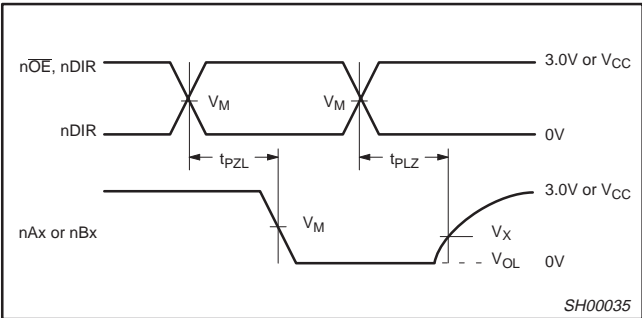
Waveform 3. Propagation Delay, nSBA to nAx or nSAB to nBx



Waveform 4. Data Setup and Hold Times



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

SWITCH POSITION

| TEST | SWITCH |
|-----------|--------|
| t_{PLZ} | closed |
| t_{PZL} | closed |
| All other | open |

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|-----------|--------------------------|-----------|-------|-------|-------|
| | Amplitude | Rep. Rate | t_W | t_R | t_F |
| 74ABT/H16 | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |

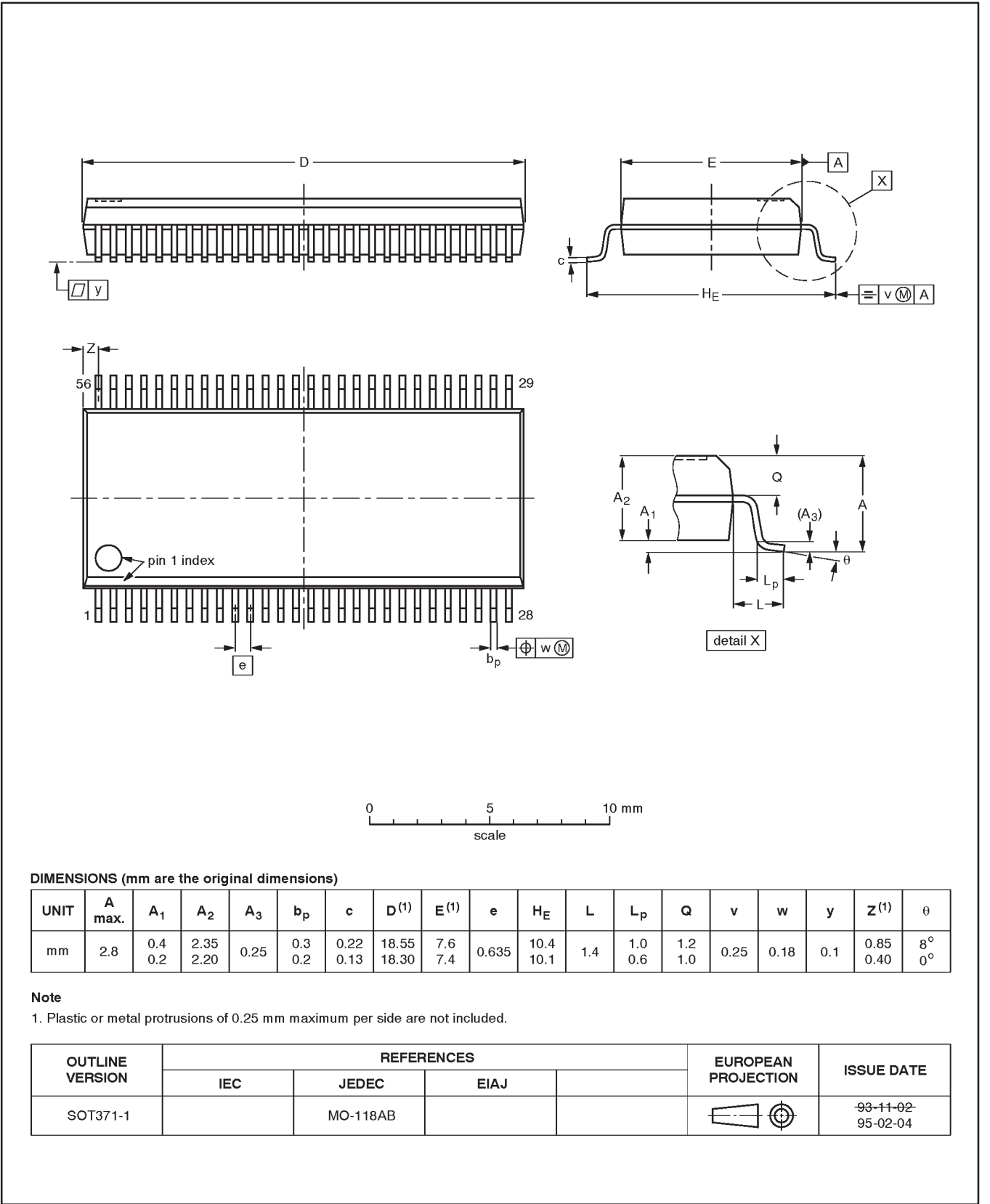
SA00018

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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

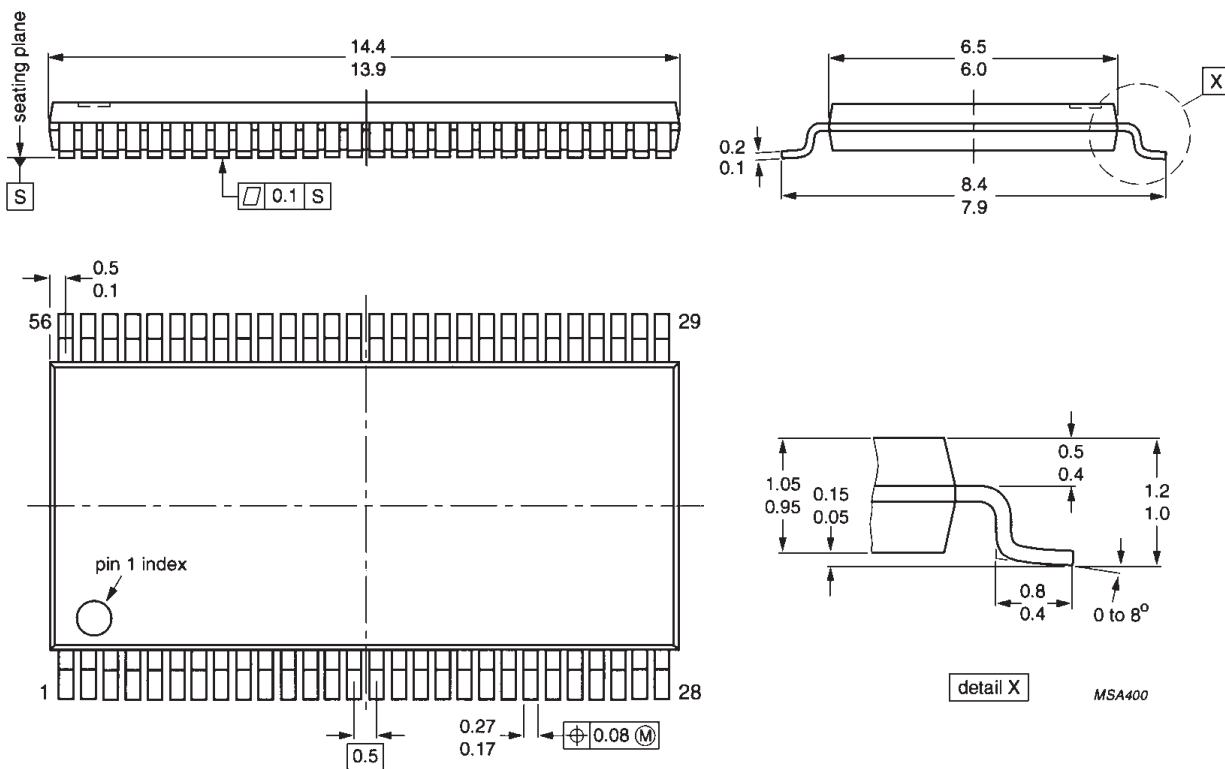


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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



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Data sheet status

| Data sheet status | Product status | Definition [1] |
|---------------------------|----------------|--|
| Objective specification | Development | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice. |
| Preliminary specification | Qualification | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification | Production | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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